Review Article

IMPLEMENTATION AND MODELING OF LOW POWER SLEEPY STACK SRAM

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Abstract: For the future technologies in which the devices and circuits are integrating more, low power consuming devices are needed. Mostly the reduction of power dissipation work is concentrated on switching and leakage current. However, sub threshold current is also a big factor which leads to power consumption especially for memories. In this paper, leakage power of SRAM memory cell is reduced by power gated sleepy stack structure which leads to lesser power dissipation. The power dissipation is reduced to 226 μW with proposed technique compared with power dissipation of conventional 6T SRAM cell which had 740 μW. With lesser power dissipation the circuit can have more battery backup and lesser heat emission

Key-words: Low Power device, Sleepy Stack, SRAM.

1. Introduction

For the VLSI circuit design, one of the top concern is power consumption of circuit. Low power consumption is not a new concern for the growing demands of application it has been a problem before mobile era. Many methodology, architecture and ideas has been proposed by researchers architecture level to device level but there is always a tradeoff between delay, area and power. So, according to the need of product or design the designer has to choose the appropriate technique [1-4]. Complementary metal oxide semiconductor (CMOS) has been used mostly for the VLSI designs. In CMOS based circuits, the power dissipation is due to switching activity which is known as dynamic component of power dissipation and static power dissipation is due to ots level (high or low). Dynamic power consumption is main concern which take dynamic power 90% of total power chip (0.18 micro meter, 0.18 μm technology and above). [5] Mostly proposed designs like frequency and voltage scaling concentrated on dynamic power dissipation [6--8]. However for shrink in feature size to 0.09 micrometre (0.09 μm) to 0.065 micro meter (0.065 μm) static power dissipation became a challenge for today's and in future technologies. Increase in subthreshold leakage power increasers dynamic power dissipation and as threshold power decreases due to scaling of circuit sub-threshold leakage power increases exponentially [9-13]. The sub threshold leakage current in nMOS is shown in figure 1.

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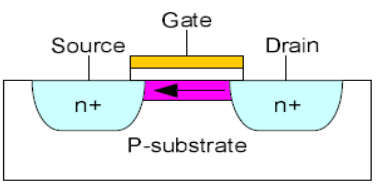

Figure 1. Subthreshold leakage of nMOS

Due to tunneling current through gate oxide insulator, gate oxide leakage power is another contributor to leakage power. [14] For nano scale gate oxide leakage is comparable to subthreshold leakage power [15-17]. For reducing this oxide leakage current high k dielctric materials can be used. For reduction in static power, sleepy stack architecture has been used in this paper, which combines advantages of two techniques i.e sleep transistor and forced stack [18-20].

2. Literature Review

2.1 Sleep Transistor

Sleep transistors are used to cut-off the supply voltage from the transistors which can be pull-up, pull-down or both with the help of self-destructive techniques [21]. A technique called MTCMOS meaning Multi- Threshold Voltage CMOS was introduced which has high threshold voltage in sleep transistors that is between the Vdd and pull-up networks and between the ground and pull-down networks. This is shown in figure 2. In order for the logic circuits to maintain high switching speeds, they use low threshold voltage transistors [22-24]. The leakage power is reduced in the sleep transistor using sleep mode by isolating them with the logic circuits. But the delay can be increased using additional sleep transistor. Due to floating values in pull-up and pull-down transistors, they lose their state in the sleep mode. The wakeup time is significantly affected due to these floating values [25].

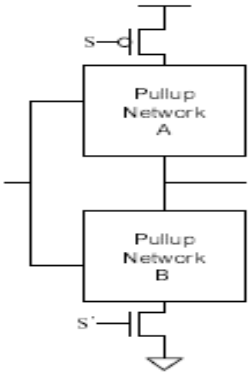

Figure 2. Sleep Transistor

2.2 Zigzag

The zigzag technique is used to reduce the cost of wakeup in sleep transistor technique. A particular state called reset is chosen to reduce the overhead of wakeup. The pull-down network is turned off for high output and when the output is high, the pull-up network is turned off. This is done for the particular circuit state [26]. The zigzag technique is shown in figure 3.

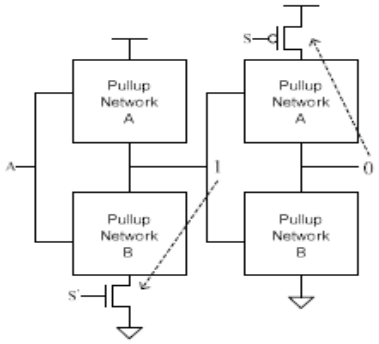

Figure 3. Zigzag Technique

2.3 Forced Stack

Transistor stacking is another technique used to reduce the leakage power. There is significant reduction in the threshold leakage current due to the stack effect when all the stacked transistors are together turned off. Figure 4 shows the forced stack inverter containing two pull-up and pull-down transistors [27].

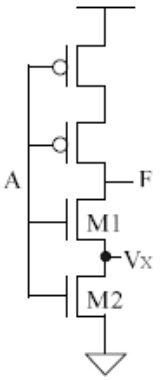

Figure 4. Forced Stack Inverter

3. Conventional 6T SRAM Cell

Figure 5 shows conventional six transistor 6T SRAM cell. The two major factors which contribute to subthreshold leakge current in this architecture are internal to cell, cell leakage current which flows from Vdd to Gnd and leakage current which flows from bitline to Gnd known as bitline leakage current [28].

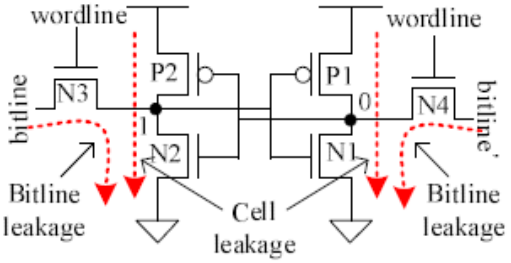

Figure 5. 6T SRAM cell

As this cell has two bitlines (bitline and bitline'), depending upon the value which is stored in SRAM cell, leakage current differs [18]. Bitline leakage accounts 35% of SRAM leakage power consumption. The total power consumption of 6T SRAM cell is 740μW.

4. Sleepy Stack Structure

The combined structure of sleep transistor technique and forced stack transistor introduces the sleepy stack structure which introduces new technique of reduction in leakage power. There are two modes in the sleepy stack technique. First one is the active mode and the other one sleep mode. The existing transistors are broken in two transistors using forced stack technique and the stack effect advantage is taken by the stack structure [299]. This is shown in figure 6. On the other hand, the existing logic circuits are isolated using the sleep transistor.

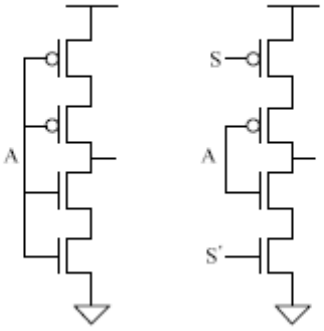

Figure 6. Stack Effect

The leakage power consumption is saved during the sleep mode using stack structure given in figure 7. It shows the sleepy stack inverter. High threshold voltage of the sleep transistors is used frequently for reduction in the leakage power. The technique of sleep transistor and stack transistor is merged in sleepy stack technique [30-31].

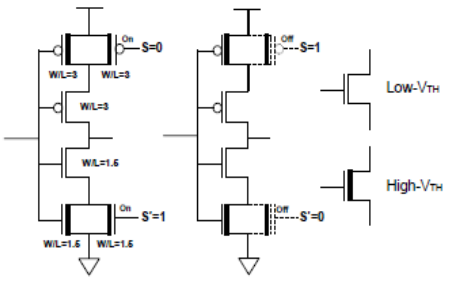

Figure 7. Stack Stack Inverter

In the active mode of sleepy stack transistor, turn on all the sleep transistors. The circuit delay can be potentially reduced in this mode [32]. Faster switching time is achieved in the active mode since all the sleep transistors are turned on. High threshold voltages can be achieved in the transistor parallel to sleep transistors as well.

In the sleep mode, the sleep transistors are turned off. The exact logic state is still maintained in the sleepy stack structure. The stack effect is induced due to turned off sleep transistors which reduces the consumption of the leakage power [33].

5. Tspice code for Sleepy Stack Structure

```
.probe
.options probefilename="U:\proj\stk11.dat"
+ probesdbfile="U:\proj\stk3.sdb"
* Main circuit: Module0
M1 ybar y N2 Gnd NMOS L=200n W=600n AD=66p PD=24u AS=66p PS=24u
M2 N6 ybar y L=200n W=600n AD=66p PD=24u AS=66p PS=24u
M3 N2 y Gnd NMOS L=200n W=200n AD=66p PD=24u M4 Gnd ybar N6 Gnd NMOS L=200n W=200n AD=66p PD=24u AS=66p PS=24u
M5 y WL BL BL AS=66p PS=24u
M7 y WL BL BL NMOS L=2u W=22u M8 N6 Gnd Gnd Gnd NMOS L=200n W=200n AD=66p PD=24u AS=66p PS=24u
M9 Gnd Gnd N2 Gnd NMOS L=200n W=200n AD=66p
M15 Vdd BLBAR N3 Vdd PMOS L=600n W=400n AD=66p PD=24u AS=66p PS=24u
v16 Vdd Gnd 5.0
v17 BL Gnd pwl(0n 5 10n 5 10.1n 0 20n 0 20.1n 5 30n 5 30.1n 0 40n 0 40.1n 5 50n 5 50.1n 0 60n 0)
v19 WL Gnd pwl(0 5 50n 5 50.1n 0 100n 0)
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6. Simulation and Results

For sleepy stack the sleepy stack technique is applied pull down and pull up transistors and to wordline transistors as shown in figure 8.

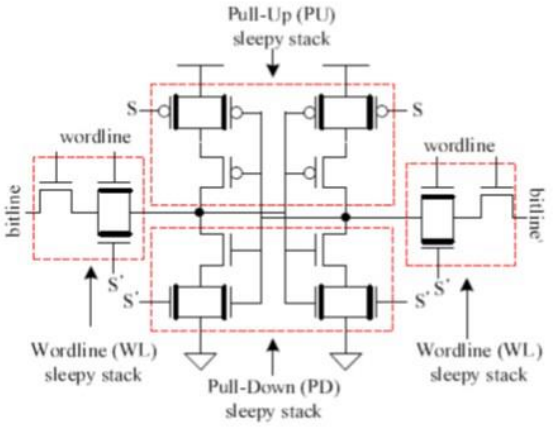

Figure 8. Wordline Transistors

The sleepy stack SRAM structure is modeled and analyzed on mentor graphic design architect tool, followed by tspice tool for power analysis. Figure 9 shows SRAM with pull up and pull down sleep stack transistor. 5V DC is provided for powering the circuit. Figure 10 shows voltage time characteristics of output y and y bar.

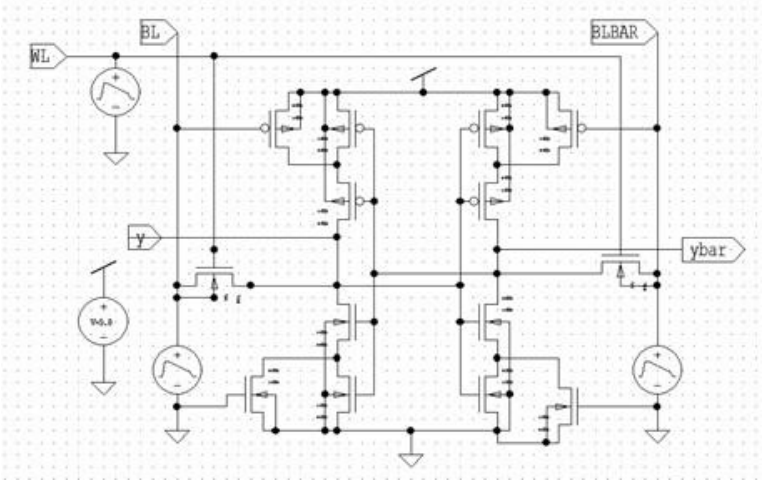

Figure 9. SRAM Structure

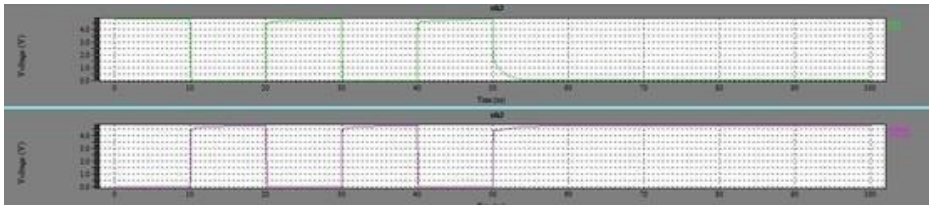

Figure 10. Voltage time characteristics

Figure 11 shows the power consumption of designed sleepy stack structure. it can be observed that total power consuption using this proposed technique is 226 μW, which was 740 μW in case of conventional 6T SRAM cell. This proposed technique has low power comsumption.

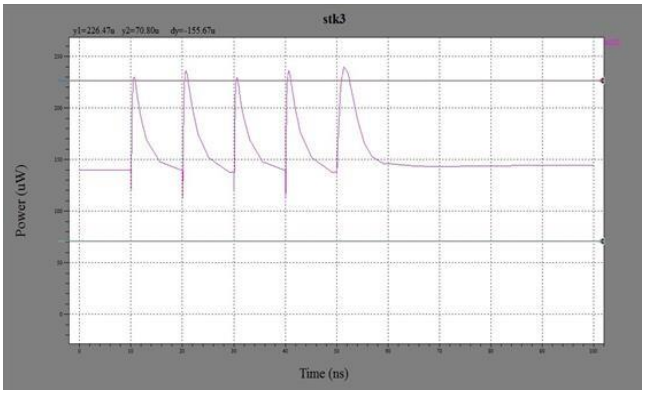

Figure 11. Power Consumption

7. Conclusion

For the requirement of low power devices, the static and dynamic components of power dissipation are reduced to make the circuit dissipate less power. This enhances the battery life of handheld devices also dissipate less heat. For reduction in static power dissipation a sleepy stacked technique is applied to SRAM cell in this paper. All the transistors Pull up 'PU", Pull down"PD" and wordline transistors are provided with sleepy stack technique which reduced the power consumption of circuit to 226 μW with same operation and applied power.

References

1. Weste, N. H., & Eshraghian, K. (1985). Principles of CMOS VLSI design: a systems perspective. NASA STI/Recon Technical Report A, 85, 47028.

2. Zhao, P., Wang, Z., & Hang, G. (2010, November). Power optimization for VLSI circuits and systems. In 2010 10th IEEE International Conference on Solid-State and Integrated Circuit Technology (pp. 639-642). IEEE.

3. Sharma, M., Singh, S., Khosla, D., Goyal, S., & Gupta, A. (2018, December). Waveguide diplexer: design and analysis for 5G communication. In 2018 Fifth International Conference on Parallel, Distributed and Grid Computing (PDGC) (pp. 586-590). IEEE.

4. Liu, D., & Svensson, C. (1994). Power consumption estimation in CMOS VLSI chips. IEEE Journal of Solid-State Circuits, 29(6), 663-670.

5. Kaur, S. P., & Sharma, M. (2015). Radially optimized zone-divided energy-aware wireless sensor networks (WSN) protocol using BA (bat algorithm). IETE Journal of Research, 61(2), 170-179.

6. Park, J. C., & Mooney III, V. J. (2006). Sleepy stack leakage reduction. IEEE transactions on very large scale integration (vlsi) systems, 14(11), 1250-1263.

7. Sharma, M., & Singh, H. (2021). Substrate integrated waveguide based leaky wave antenna for high frequency applications and IoT. International Journal of Sensors Wireless Communications and Control, 11(1), 5-13.

8. Sharma, M., & Singh, H. (2018, December). SIW based Leaky wave antenna with Semi C-shaped slots and its Modeling, Design and parametric considerations for different materials of Dielectric. In 2018 Fifth International Conference on Parallel, Distributed and Grid Computing (PDGC) (pp. 252-258).

9. Sreekala, K. S., & Krishnakumar, S. (2016, October). Subthreshold leakage power reduction by feedback sleeper-stack technique. In 2016 International Conference on Emerging Technological Trends (ICETT) (pp. 1-7).

10. Gupta, A. K., Sharma, M., Khosla, D., & Singh, V. (2020). Object detection of colored images using improved point feature matching algorithm. Central Asian Journal of Mathematical Theory And Computer Sciences, 1(1), 13-16.

11. Park, J. C., Mooney, V. J., & Pfeiffenberger, P. (2004, September). Sleepy stack reduction of leakage power. In International Workshop on Power and Timing Modeling, Optimization and Simulation (pp. 148-158). Springer, Berlin, Heidelberg.

12. Kaur, N., & Sharma, M. (2017, August). Brain tumor detection using self-adaptive K-means clustering. In 2017 International Conference on Energy, Communication, Data Analytics and Soft Computing (ICECDS) (pp. 1861-1865). IEEE.

13. Pal, P. K., Rathore, R. S., Rana, A. K., & Saini, G. (2010, September). New low-power techniques: Leakage feedback with Stack & Sleep stack with keeper. In 2010 International Conference on Computer and Communication Technology (ICCCT) (pp. 296-301). IEEE.

14. Gupta, A. K., Sharma, M., Sharma, A., & Menon, V. (2020). A Study on SARS-CoV-2 (COVID-19) and Machine Learning Based Approach to Detect COVID-19 Through X-Ray Images. International Journal of Image and Graphics, 2140010.

15. Islam, M. S., Nasrin, M. S., Mansur, N., & Tasneem, N. (2010, December). Dual stack method: A novel approach to low leakage and speed power product VLSI design. In International Conference on Electrical & Computer Engineering (ICECE 2010) (pp. 89-92). IEEE.

16. Sharma, M., & Gupta, A. K. (2021). An Algorithm for Target Detection, Identification, Tracking and Estimation of Motion for Passive Homing Missile Autopilot Guidance. In Mobile Radio Communications and 5G Networks (pp. 57-71). Springer, Singapore.

17. Narayan, S. L., Korah, R., & Kumar, N. K. (2013, April). A novel sleepy stack 6-T SRAM cell design for reducing leakage power in submicron technologies. In 2013 International Conference on Communication and Signal Processing (pp. 753-757). IEEE.

18. Sharma, M., Sharma, B., Gupta, A. K., & Singla, B. S. (2020, March). Design of 7 GHz Microstrip Patch Antenna for Satellite IoT-and IoE-Based Devices. In The International Conference on Recent Innovations in Computing (pp. 627-637). Springer, Singapore.

19. Sri, B. S., Saraswathi, B., Kumar, G. A., & Singh, A. B. (2012). Design of Low Power 4-Bit Full Adder Using Sleepy Keeper Approach. International Journal of Research in Engineering and Technology, 1(03), 355-358.

20. Singh, S., Sharma, M., Khosla, D., Palta, P., Gupta, A. K., Sharma, T., & Goyal, S. (2019, October). A Novel Approch for Deblurring Colored Images using Blind Deconvolution Algorithm. In 2019 5th International Conference on Signal Processing, Computing and Control (ISPCC) (pp. 108-113). IEEE.

21. Khosla, D., Sharma, M., Khanna, S. K., Khanna, P., & Kaur, G. (2019). Smart Robotic Arm. Journal of Artificial Intelligence Research & Advances, 6(2), 58-62.

22. Nowak, E. J., Rainey, B. A., Fried, D. M., Kedzierski, J., Ieong, M., Leipold, W., ... & Breitwisch, M. (2002, December). A functional FinFET-DGCMOS sram cell. In Digest. International Electron Devices Meeting, (pp. 411-414). IEEE.

23. Khosla, D., Sharma, M., Sharma, A., Budhiraja, A., & Singh, S. (2019). Blockchain based supply chain management: an overview. Int. J. Control Automat, 12(5), 424-430.

24. Sreekala, K. S., & Krishnakumar, S. (2016, October). Subthreshold leakage power reduction by feedback sleeper-stack technique. In 2016 International Conference on Emerging Technological Trends (ICETT) (pp. 1-7). IEEE.

25. Singh, S., Singla, B. S., Sharma, M., Goyal, S., & Sabo, A. (2021). Comprehensive Study on Internet of Things (IoT) and Design Considerations of Various Microstrip Patch Antennas for IoT Applications. In Mobile Radio Communications and 5G Networks (pp. 19-30). Springer, Singapore.

26. Swaroop, V. S., Krishna, B. M., & Bhaskar, M. V. (2012). DESIGN OF LOW POWER 8 BIT SRAM ARCHITECTURE USING LEAKAGE FEED BACK WITH STACK & SLEEP STACK WITH KEEPER. International Journal of Engineering Research and Apllication (IJERA), 2(2), 192-201.

27. Gupta, A. K., Sharma, M., Singh, S., & Palta, P. (2020). A Modified Blind Deconvolution Algorithm for Deblurring of Colored. Advances in Computational Intelligence Techniques, 157.

28. Saini, P., & Mehra, R. (2012). Leakage power reduction in CMOS VLSI circuits. International Journal of Computer Applications, 55(8).

29. Kakkar, R., Singh, S., Singh, J., Goyal, S., Khosla, D., & Sharma, M. (2020, March). Investigations on Mathematical Modeling of Imaging Infrared (IIR) Missile. In The International Conference on Recent Innovations in Computing (pp. 381-390). Springer, Singapore.

30. Chun, J. W., & Chen, C. R. (2010, November). A novel leakage power reduction technique for CMOS circuit design. In 2010 International SoC Design Conference (pp. 119-122). IEEE.

31. Singla, B. S., Sharma, M., Gupta, A. K., Mohindru, V., & Chawla, S. K. (2020, March). An Algorithm to Recognize and Classify Circular Objects from Image on Basis of Their Radius. In The International Conference on Recent Innovations in Computing (pp. 407-417). Springer, Singapore.

32. Sharma, M., Pandey, D., Palta, P. et al. Design and Power Dissipation Consideration of PFAL CMOS V/S Conventional CMOS Based 2:1 Multiplexer and Full Adder. Silicon (2021). https://doi.org/10.1007/s12633-021-01221-1.

33. Gupta, P., & Kumar, M. (2018). Design of modified low power CMOS differential ring oscillator using sleepy transistor concept. Analog Integrated Circuits and Signal Processing, 96(1), 87-104.